groove or trench **34** is formed to extend downward from a surface of the source layer **24** so as to penetrate through the source layer **24** and the base layer **23** and to reach an internal portion of the drain layer **22**. A trench inner wall portion of the base layer **23** constitutes a channel region.

A gate oxide film **25** is formed to cover an inner wall surface of the trench **34** and to extend on a trench peripheral surface portion of the source layer **24**, and a gate electrode **26** is formed on the gate oxide film **25**. In addition, an interlayer insulator film **27** is formed on the gate electrode **26**. A side insulator film **30** is formed on the source layer **24** so as to cover each side end surface of the gate electrode **26**. This side insulator film **30** is different from the interlayer insulator layer **27**.

A contact hole **33** is formed in the substrate to have an inner wall surface in alignment with an outer surface of the side insulator film **30**, namely, in a self-alignment manner. This contact hole **33** is filled with a tungsten electrode **29** which is used for application of a back gate bias voltage. Therefore, this tungsten electrode **29** is in electrical contact with the source layer **24** and the base layer **23**. A source electrode **28** is formed to extend over the interlayer insulator film **27** and in electrical contact with the tungsten electrode **29**.

Now, a process for manufacturing the vertical power field effect transistor shown in FIG. **3** will be explained with reference to FIGS. **4A** to **4F**.

A silicon layer is epitaxially grown on the N-type silicon substrate **21**, and doped with impurity so as to form the N-type drain layer **22**. The P-type base layer **23** is formed by diffusing P-type impurity into a surface of the drain layer **22**, and the N-type source layer **24** is formed by diffusing N-type impurity into the base layer **23**. These impurity diffusions can be performed by a photoresist process, an ion implantation or a thermal diffusion. Thus, as shown in FIG. **4A**, the drain layer **22**, the base layer **23** and the source layer **24** are formed on the N-type silicon substrate **21**.

Thereafter, the trench **34** is formed in the substrate **21** by a photoresist process and a anisotropic etching, and then, an gate oxide film **25** is formed, a polysilicon layer (becoming the gate electrode) is deposited, and an interlayer insulating film **27** of an oxide film is formed, as shown in FIG. **4B**.

As shown in FIG. **4C**, these layers are selectively removed by a photoresist process, and thereafter, as shown in FIG. **4D**, an oxide film **31** is grown on a whole surface.

Then, the oxide film **31** is anisotropically etched to the effect that the oxide film **31** remains only on each side surface of the gate electrode **26** and the other oxide film is completely removed. The oxide film **31** remaining on each side surface of the gate electrode **26** forms the side oxide film **30**, as shown in FIG. **4E**.

Thereafter, as shown in FIG. **4F**, a resist mask **32** is formed on the interlayer insulator **27**. In this connection, it is not necessarily required that a pattern of the resist mask **32** is completely in matching with or in alignment with the pattern of the interlayer insulator film **27**, and therefore, the resist mask **32** is allowed to overlap the side oxide film **30** to some degree. An anisotropic etching is performed by using the side oxide film **30** as a mask, so as to form a contact hole **33** in self-alignment with the gate electrode **26**, as shown in FIG. **4F**.

Thereafter, the resist mask **32** is removed, and tungsten is filled into the contact hole **33** so as to form the tungsten electrode **29** in self-alignment with the gate electrode **26**. Then, the source electrode **28** is formed by an evaporation or a photoresist process. Thus, the vertical power field effect transistor is completed as shown in FIG. **3**.

For example, if in the conventional process for the rectangular-grooved vertical power MOS field effect transistor, the margin for alignment in the photoresist process is 0.5 μm, and the margin for the side etching is 1.0 μm, the lateral cell size can be reduced by 3.0 μm. For example, in the case of the vertical power MOSFET having the breakdown voltage of 60 V, the base region width can be reduced from 10 μm to 7 μm or less, and therefore, can be improved by about 30%.

The above mentioned embodiments have been the N-channel vertical power MOSFET. However, in the embodiments shown in FIGS. **1** and **3**, if the P-type regions or layers are changed into N-type regions or layers and the N-type regions or layers are changed into P-type regions or layers, it is of course possible to constitute the P-channel vertical power MOSFET.

The invention has thus been shown and described with reference to the specific embodiments. However, it should be noted that the present invention is in no way limited to the details of the illustrated structures but changes and modifications may be made within the scope of the appended claims.

We claim:

1. A method for manufacturing a vertical power field effect transistor comprising the steps of:

forming a first insulating film covering on a principal surface of a semiconductor substrate of a first conductivity type;

forming a conducting layer on said first insulating film;

forming a first interlayer insulating film covering said conducting layer;

patterning a stacked structure formed of said first insulating film, said conducting layer and said first interlayer film so as to form a patterned stacked structure and to expose a portion of said substrate uncovered by said patterned stacked structure, said first insulating film of said patterned stacked structure forming a gate insulator film, said conducting layer of said patterned stacked structure forming a gate electrode;

introducing an impurity of a second conductivity type opposite to said first conductivity type into said exposed portion of said substrate by using the patterned stacked structure as a mask, so that a base region extending under said gate electrode is formed;

introducing an impurity of said first conductivity type by using the patterned stacked structure as a mask, so that a source region smaller than said base region is formed in said base region and extends under said gate electrode;

forming a second interlayer insulating film on said principal surface of said substrate;

anisotropically etching said second interlayer insulating film so as to form a side insulating film which covers only each side surface of the gate electrode and the gate insulator film;

anisotropically etching said substrate by using the side insulating films as a mask, so as to form, in a self-alignment manner, a groove which extends downward from said principal surface of said silicon substrate to pass through said source region and to reach said base region;